SUMMARY
We have investigated fabricating fine active regions by tuning process condition of conventional LOCOS for the fabrication of the gate width 100 nm MOSFET. Considering the lowering in fluidity of silicon dioxide, oxidation temperature was changed to 900°C which is lower than conventional 1000°C. In addition active region shape was modified to utilize vertical stress due to nitride elastic force. As a result, 75 nm width fine active region was successfully fabricated. Though lowering of the oxidation temperature tends to increase stress, junction leakage current and gate oxide reliability showed no degradation. On the other hand, PSL (Poly-Si Sidewall LOCOS) gave rise to degradation in the electrical properties by the stress. Using the LOCOS process, we have fabricated the MOSFETs with the fine active regions.

1. Introduction
We have investigated fabrication of MOSFETs with ultra-small active regions. In this report we focus to fabrication issues although we aim to evaluate characteristics fluctuations in the ultra-small area MOSFETs. Based on the scaling theory gate length has been shrunken actively. Gate width shrinking is also necessary for high density integration [1]. The MOSFET gate width is defined by an isolation structure. LOCOS has been the most popular isolation method. Although STI (Shallow Trench Isolation) is currently used for mass production of advanced devices [2], simple process of LOCOS is still attractive. Lateral oxide encroachment during oxidation (bird’s beak) is the obstacle for controlling the gate width with the LOCOS technique. Modification of LOCOS process to suppress bird’s beak encroachment sometimes degrade device reliability because of oxidation induced stress [3], [4]. We have applied the LOCOS technique for the fabrication of 100 nm width MOSFETs paying attention to such side effects.

2. Experimental Procedures
To suppress bird’s beak encroachment, we modified the field oxidation temperature and the active region shape. As a field oxidation temperature, we selected 900°C and 1000°C (Fig. 1). Since oxide viscosity becomes very high for the temperature lower than about 950°C [5], [6], we prospected to appear variation in field oxide shape at isolation edges by lowering the oxidation temperature from conventional 1000°C to 900°C. We considered that the modification of the active region shape would be helpful for the bird’s beak suppression because the encroachment length depends on the active area width. Therefore we designed the H-type test structure shown in Fig. 2 for bird’s beak encroachment evaluation in addition to a conventional L/S structure. The H-type structure is constructed with wide region and narrow region whose length and width are 0.5 µm and \( W \) (\( W \): 0.05 µm to 2 µm), respectively.

PSL (Poly-Si Sidewall LOCOS) [7] (Fig. 3) is also evaluated for comparison. A lot of modified LOCOS were proposed such as SSS-OSELO (Single-Si\(_3\)N\(_4\)-Spacer-Offset LOCOS).
COS) [8], PBL (Poly-Si Buffered LOCOS) [9] and PSL. We have evaluated PSL in addition to conventional LOCOS, because PSL is expected to prevent field oxide thinning at isolation edges and degradation of gate oxide reliability.

In order to evaluate the influence of the modification to an isolation structure we fabricated MOS diodes and n+p junction diodes. After formation of LOCOS or PSL on Si (100) substrates, BF$_2$ ion was implanted into active region at 30 keV and 140 keV with a dose of 6×10$^{12}$ cm$^{-2}$ and 1×10$^{13}$ cm$^{-2}$, respectively. Channel stop was carried out through the field oxide by B$^+$ ion implantation at 85 keV with a dose of 5×10$^{12}$ cm$^{-2}$. Gate oxide thickness for the MOS diodes were 2 nm. N$^+$ region for the n+p junction diodes were formed by RTA with 900˚C 10 sec after arsenic ion implantation at 20 keV with a dose of 5×10$^{15}$ cm$^{-2}$.

3. Result and Discussion

Cross-sectional SEM views of field oxide temperature for the oxidation of 900˚C and 1000˚C are shown in Fig. 4 and Fig. 5, respectively. Oxidation time to grow 150 nm field oxide at 1000˚C and 900˚C is 22 min and 130 min, respectively. The active region width, in other words nitride width, is about 100 nm. Increase in the pad oxide thickness is clearly observed other than the specimen with the H-type shape and oxidized at 900˚C. For the specimens in these figures, nitride and initial pad oxide thicknesses are 115 nm and 5 nm, respectively. Therefore total thickness indicated by vertical arrows in these figures are ideally 120 nm. The relationship between the nitride width and pad oxide thickness is shown in Fig. 6. It is shown that H-type is better than L/S and 900˚C is better than 1000˚C from the magnitude of the pad oxide thickness increase. In the case of PSL a bump to avoid a hollow at the isolation edge is not obvious in an SEM image (Fig. 7). Since the large bump is an obstacle for the following process, the result shown in Fig. 7 is adequate. The minimum active region width with PSL where no pad oxide thickness increase was found was 145 nm for the oxidation temperature of 900˚C and H-type mask. PSL seems to be inferior to the conventional LOCOS for the suppression of bird’s beak encroachment.

The diffusion coefficient of oxidant in pad oxide film is
smaller than that in field oxide film because of stress [10]. The H-type structure is considered to work for increasing the stress in pad oxide film by the following mechanism. The H-type structure consists of a narrow active region and wide square regions those sandwiches the narrow region from its longitudinal direction. As the oxidation progresses, edge portion oxide thickness becomes thicker than inside portion of the active region. In case that the test structure consists a narrow line only, the entire silicon nitride mask is lifted by grown pad oxide and stress enhancement is not expected. However, in the H-type structure, since oxidation at the inside of the wide square region is negligible compared with the edge portion, bending stress is enhanced in the silicon nitride. As results of the bending stress and elastic force of the silicon nitride film, the compressive stress in pad oxide film becomes large. Therefore, oxidation in the pad oxide is suppressed because of stress induced oxidant diffusion reduction.

Based on previously shown results, n’/p junction diodes were fabricated. Junction diode pattern was designed as shown in Fig. 8 using the H-type shape to evaluate the influence of narrow active regions. The perimeter length of isolation edge for narrow active regions was 30% to 50% of the entire perimeter length. Figure 9 shows weibull plots as a function of diode leakage current at reverse bias voltage of 1.5 V measured with 24 diodes. No significant difference is found between oxidation temperatures of 900˚C and 1000˚C while PSL results in large defect frequency. We evaluate the diodes with 3 times longer perimeter also, and weibull distribution is not degraded. Therefore we believe that the junction failure at the LOCOS distribution tail is originated from processes other than LOCOS. Empty circle in Fig. 10 shows measured leakage current Imeasured at reverse bias voltage of 1.5 V against nitride width W for oxidation temperature of 900˚C. Though the leakage current increases as W becomes smaller in Fig. 10 it is apparent increase and it does not originate from stress induced defects. It is due to the intricate relationship between the area and the perimeter length of diode pattern shown in Fig. 8. To interpret this result into a simple relationship, the perimeter and the area dependent components of the current were extracted assuming the relationship

\[ I_{FIT} = AJ_a + LJ_p \]  

(1)

Where \( I_{FIT} \) is normalized total current, \( A \) is area, \( L \) is perimeter length, \( J_a \) is the area components of the current. \( J_p \) is perimeter components of the current. The solid line in Fig. 10 represent the calculated \( I_{FIT} \) using the extracted \( J_a \) and \( J_p \). The solid circles in Fig. 10 represent ratio of measured leakage current \( \frac{I_{measured}}{I_{FIT}} \) \( \frac{I_{measured}}{I_{FIT}} \) does not show \( W \) dependence, this indicates that increase in leakage current in the narrow active cases due to the stress induced defects is negligible.

Figure 11 shows TDDB (Time Dependent Dielectric Breakdown) characteristics of MOS diodes fabricated with the LOCOS for the fine active area formation. The TDDB characteristics was obtained with a constant voltage stress of –3.8 V. Open circles and solid circles in the figure represent

\[ \text{Fig. 8 Plan view layout of a diode designed with the H-type structure consisting narrow active regions.} \]

\[ \text{Fig. 9 Leakage current of n’/p junction diodes at reverse bias voltage of 1.5 V.} \]

\[ \text{Fig. 10 Measured leakage current of n’/p junction diodes } I_{measured} \text{ normalized current } I_{FIT} \text{ and there ratio } \frac{I_{measured}}{I_{FIT}} \text{ as a function of mask width } W. \text{ The definition of } I_{FIT} \text{ is described with Eq. (1).} \]
MOS diodes with short and long isolation perimeter, respectively. Although the ratio of perimeter lengths is nearly five, no difference is observed. Therefore we can conclude that the LOCOS process for the fine active area has no bad effect to gate oxide reliability.

The plan view SEM image of a fabricated MOSFET is shown in Fig. 12. We fabricated MOSFETs whose gate length and width are nearly 100 nm. As $I_D-V_D$ characteristics and $I_D-V_G$ characteristics shown in Figs. 13 and 14, the MOSFETs were successfully fabricated.

4. Conclusion

We have investigated fabricating fine active regions by improving LOCOS process condition. We changed field oxidation temperature to 900°C from 1000°C to suppress the bird's beak encroachment by the lowering in fluidity of silicon dioxide. We used the H-type active region shape to utilize vertical stress due to elastic force by the nitride mask. As a result, 75 nm width active region was successfully fabricated. In spite of possible increase in stress, the junction leakage current characteristics and the reliability showed no gate oxide degradation. Based on this we have fabricated the MOSFETs with fine active regions by the simple LOCOS process.

This work does not directly mean that LOCOS is useful for sub-100 nm narrow MOSFET fabrication. For example, H-type structure contains area penalty problem. However, this paper describes the possibility of LOCOS technology as a test base for narrow MOSFET characteristics.

References


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