The Development of UWB Gaussian Monocycle Pulse Synchronization Circuit

based on 0.18-µm CMOS Technology

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1. Introduction
RF wireless clock/data transmission using integrated antenna, capacitor or inductor is the newly developed technology for intra/inter-chip interconnection in future ULSI [1][2]. As for data transmissions among stacked ULSI modules (Fig.1) [3], both high data transmission rate and multi-channel accessibilities are required. UWB (Ultra-Wide-Band) technology is one of the solutions of this problem [4]. The goal of the research is the development of 1Gbps, single-chip, and CMOS UWB transceiver using Gaussian monocycle pulse (GMP) as a transmitted waveform [5]. In the receiver side, amplifier and demodulator, which is based on pulse correlation method, have been already developed, and measurement results will be presented in IWUWB 2005. However, the synchronization between transmitter and receiver remains as an unsolved problem. In this paper, GMP synchronization scheme is verified using MATLAB/Simulink simulation, and circuit level simulations by HSPICE are also shown.

2. Synchronization Scheme
The block diagram of the proposed synchronization circuit is shown in Fig. 2. The synchronization scheme consists of two steps, i.e., (i) phase synchronization and (ii) frequency synchronization. The circuit receives the following GMP \( r(t) \), which is the first derivative of Gaussian.

\[
r(t) = -\left(\frac{2\pi t}{\tau}\right)e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2}
\]

(1)

Here \( \tau \) denotes the pulse width of GMP. Mixer and integrator circuits give the correlation between the received signal \( r(t) \) and template signal \( v_1(t) \). Here \( v_1(t) \) should have the same waveform as \( r(t) \). The phase of \( v_1(t) \) is shifted until the value of the correlation exceed the threshold \( V_{th} \).

\[
\int_{-\tau}^{\tau} r(t) \cdot v_1(t - \Delta t) dt = \begin{cases} \geq V_{th} \to \Delta t_{i+1} = \Delta t_i + \Delta t_{locked} \\ < V_{th} \to \Delta t_{i+1} = \Delta t_i + \delta t \end{cases}
\]

(2)

Here \( \delta t \) is the unit delay, and \( \Delta t \) shows the amount of time shift. After phase synchronization, frequency synchronization is performed. The second derivative of Gaussian is given as another template signal \( v_2(t) \).

\[
v_2(t) = \left(\frac{2\pi t}{\tau}\right)^2 - 1 \cdot e^{-\frac{1}{2}\left(\frac{2\pi t}{\tau}\right)^2}
\]

(3)

Another correlation circuit performs the correlation between \( r(t) \) and \( v_2(t) \). The output voltage \( \Delta V_{LO} \) is used to control the repetition frequency of the local oscillator \( f_{LO} \).

\[
\Delta V_{LO} \propto \int_{-\tau}^{\tau} r(t) \cdot v_2(t - \Delta t_{locked}) dt
\]

(4)

Here an orthogonality relation between \( r(t) \) and \( v_2(t) \) is used.

3. Circuit Design and Simulation
Above synchronization algorithm is verified using MATLAB/Simulink calculation. Figure 3 is the results of Simulink simulation. Where the repetition frequency of synchronization circuit is given as 1GHz, and the difference of the repetition frequency between transmitter and receiver is assumed as 1MHz. The center frequency of GMP is 5GHz. In this condition, the unit delay of DLL should be at least less than the pulse width of GMP (=0.2ns). This time, 1GHz, differential 8 stages VCO, which can generate different 16 phases, is designed and simulated. Corresponding unit delay is about 63ps. This value satisfies above requirement. Whole circuit layout of the phase synchronization circuit, which is developed using TSMC CMOS 0.18-µm process, is given in Fig 4. The schematic diagram of the delay cell of this ring oscillator is given in Fig 5 (a). HSPICE result of the VCO is shown in Fig. 6. (a). Repetition frequency becomes 960MHz. After 8 to 1 differential multiplexer, a part of its schematic is shown in Fig. 5. (b), repetition frequency downs to 790MHz.

Figure 5. (c) shows a schematic of the 4 bit counter, which is used as the delay controller. Simulation results are given in Fig. 6. (b).

4. Summary
The new synchronization scheme for Gaussian monocycle pulse was developed. MATLAB/Simulink results indicate that delay cells at least below 200ps are necessary. HSPICE simulation of phase synchronization circuit was demonstrated. The VCO repetition frequency after multiplexer was 790MHz.

References
Fig. 1. Conceptual figure of inter-chip wireless interconnections using integrated dipole antennas.

Fig. 2. The block diagram of the proposed synchronization circuit.

Fig. 3. Simulation results of synchronization scheme using MATLAB/Simulink.

Fig. 4. Chip layout of synchronization circuit.

Fig. 5. Schematic diagram of (a) 8 stages VCO delay cell. (b) 2 to 1 multiplexer. (c) 4bit counter.

Fig. 6. HSPICE results. (a) VCO output (repetition frequency 960MHz). (b) 4bit counter output.
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Wireless Inter-chip Interconnection
Signal Delay Due to RC → Serious Problem for Future ULSI
Solutions
• Copper/low-k Interconnection → Limitation from Materials
• RF Wireless Technology → Re-configurable Interconnection
Goal
• Development of On-Chip Wireless Interconnections for High Speed Clock/Data Transmission.
• Pulse-based UWB → Multiple Accessibility

Target Performance
• Single Chip
• 1Gbps Data Rate (Single Channel)
• Target Distance : 1mm ~ 1cm

Synchronization Algorithm
1. Phase Synchronization
• Received signal \( r(t) \): Gaussian Monocycle Pulse
  \[ r(t) = \left( \frac{2\pi f}{T} \right)^{-\frac{1}{2}} \exp \left( -\frac{1}{2} \left( \frac{t}{T} \right)^2 \right) \]

2. Frequency Synchronization using orthogonality
• Received signal \( r(t) \): Gaussian Monocycle Pulse
  \[ v_f(t) = \left( \frac{2\pi f}{T} \right)^{-\frac{1}{2}} \exp \left( -\frac{1}{2} \left( \frac{t}{T} \right)^2 \right) \]

Goal
• Developed Pulse-based UWB

Previous Achievements
• Pulse-based UWB → Multiple Accessibility

Improvement of Receiver
Previous Circuit
• Succeeded in the demodulation of OOK modulated Gaussian Monocycle Pulse
• LNA output was used as template signal to avoid the synchronization problems

Improvement
• Development of synchronization circuit for Gaussian Monocycle Pulse (GMP)
  1. Phase synchronization
  2. Frequency synchronization

Circuit Block Diagram

MATLAB Simulation

Phase Synchronization Circuit

Differential VCO

Summary
• The new synchronization scheme for Gaussian monocycle pulse was developed.
• MATLAB/Simulink results indicate that delay cells at least below 200ps are necessary.
• HSPICE simulation of phase synchronization circuit was demonstrated. The VCO repetition frequency after multiplexer was 790MHz.

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