Low-Power Digital Image Segmentation of Real-Time VGA-Size Motion Pictures


Introduction

(1) Image-Segmentation Purpose
- Partitioning of natural images into meaningful regions
- Initial task for enabling higher-level image processing

(2) Necessary Hardware-Implementation Features
- Low-power-dissipation circuitry for mobile applications
- Pixel-parallel processing for real-time segmentation of motion pictures

Outline of Digital Segmentation Algorithm

1. Weight calculation: Difference of luminance between pixels
2. Leader cell selection: Sum of weights with neighboring pixels has to be larger than a threshold
3. Segmentation: Repeat self-excitation, excitation, and inhibition

Cell-Network

- Consists of registers and adders/subtractors
- Changes its state \( x_k \in \{0, 1\} \) depending on \( \sum W_{ik} \times x_k \) of 8 neighbors

Weight-register block (WRB): Two register-block types (horizontal/vertical)
- Store the 4 connection-weights between the adjacent active cells
- Output weights \( W_{ik} \times x_k \) to adjacent active cells

Cell-Network can be implemented by alternately laying an active cell and a WRB
- Area minimization with effective sharing of WRBs among neighboring cells
- High speed execution by pixel-based fully parallel processing

Segmentation Time: 9.5\( \mu \text{sec} \) (worst)

Power Dissipation (3.3V): 24.4mW@10MHz (ave.)
26.4mW@10MHz (worst)

Measured Max Frequency: 25MHz

Transistors: 249,810

Pixel Integration Density: 19.6pixel/mm²
High-Speed Architecture (Weight Parallel, WP)
- 90nm CMOS with 5 routing layers
- For 320 × 240 (QVGA) image
- Processing Time: < 250 µsec at 10MHz
- Chip-size: < 116mm² (11mm × 11mm)
- Typical chip-size for cost-performance market in 2004 is expected at 195mm² from ITRS2002 Update

High-Density Architecture (Weight Serial, WS)
- 90nm CMOS with 5 routing layers
- For 320 × 240 (QVGA) image
- Chip-size: < 62mm² (8mm × 8mm)

Boundary-Active-Only Scheme (BAO)
- State-transition evaluation is only necessary for the grown regions boundary cells
- (Only boundary cells are in active mode and other cells are in stand-by mode)
- More than 75% power reduction is achieved for the 10 × 10 pixel cell-network
- Without BAO
  - Average: 38.4mW
  - Worst: 38.9mW
- With BAO
  - Average: 6.81mW
  - Reduction: 78.2%
- Without BAO
  - Average: 30.9mW
  - Worst: 38.9mW
- With BAO
  - Average: 6.81mW
  - Reduction: 78.2%

Global inhibitor ZOR
- Calculates an OR function of the active mode-status signals of all cells
- If there are cells in active mode, this circuit outputs a "1" (ZORi = 1)
- The region-growing boundary is partly determined by ZORi for each row
- There are state transitions in row 3. During the next clock-cycle, rows 2, 3, 4 have possibilities that state transition cells exist!
- Clock control for each row:
  - Only region-growing boundary rows are activated by gated clock signal
  - The activated rows are determined from the ZORi signals

Subdivided-Image Approach (SIA)
- Segmentation time of the proposed segmentation architecture is much faster than required, so sequential processing becomes possible

Chip-size estimation
(Estimated from full-custom layout with 3 metal layers 350nm CMOS technology)

Processing Time
- (Estimated from full-custom layout with 3 metal layers 350nm CMOS technology)

Total processing time: 7.49msec
- Estimated segmentation time: 23.1 µsec
- Estimated power dissipation: 28.0mW

Subdivided images
- 16 blocks
- VGA-size (640×480 pixels) image
- 15 blocks
- Pipeline processing
- Segmenting: (16 × 15) blocks × 23.1 µsec = 5.52msec
- Data in/out: (16 × 15) blocks × 0.1 µsec = 2.46msec (at 10MHz clock frequency)
- Total processing time: 7.49msec

LSI
- restores segmented image
- processed block overlapping (41 × 33 pixels) area (1 pixel)