Associative Memory for High-Speed Nearest Hamming/Manhattan Distance Search with Large Reference Pattern Number

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**Associative Memory Functionality**

- Finding the nearest match pattern among R reference patterns.
- Important for pattern recognition (Hamming) and codebook based data compression (Manhattan).
- Minimum Hamming distance search for pattern recognition with binary (black/white) images.
- Manhattan distance for many applications with color/gray-scale images.

**Input Pattern**

- Reference Patterns
  - Index of Most Similar Pattern
  - Hamming Distance Search
  - Minimum Distance Search
  - Distance Calculation

**Ex. 1: Image Pattern Recognition**
- Input Image
  - English Character Database
  - Output C

**Ex. 2: Codebook Based Image Compression**
- Input Vectors
  - Codebook (4 x 4 pixels)
  - Outputs
  - Match Line

**Associative Memory Architecture**

- K-bit subtractors and absolute value calculators (UC, WC) within the memory field.
- A fast and static analog-current-encoding of the word-comparison results.
- Improved self-adapting regulation circuit to the point of the largest winner-loser distance amplification for all search cases.
- Winner search circuit (WLA, WTA) with only O(R) complexity.

- Each stage amplifies the differences by a voltage-current-voltage transformation.
- Enough amplification magnitude (by a factor 20-50).

- The current on \( C_{\text{win}} \) is the smallest and the voltage of \( C_{\text{win}} \) is the lowest.
- The current-source capability of \( P_{\text{win}} \) is the largest and the voltage of \( LA_{\text{win}} \) is the highest.
- The feedback voltage of F is approximately equal to that of \( C_{\text{win}} \).
- For larger winner-input distance the voltage F becomes higher and \( n_{\text{win}} \) have larger current-sink capability.

**Search Word (W bit)**

- SC1, SC2, SC3, SC4
- UC1, UC2, UC3, UC4
- WC1, WC2, WC3, WC4
- SCW1, SCW2, SCW3, SCW4
- UCW1, UCW2, UCW3, UCW4
- RW1, RW2, RW3, RW4
- Match Signals

- Winner Line-Up Amplifiers (WLA)
- Winner Take All Circuit (WTA)
- Match Signals

- 1st WTA Stage
- 2nd WTA Stage
- 3rd WTA Stage
- 4th WTA Stage
- 5th WTA Stage
- Decade Circuit
**Conclusions**

- **Associative memories without and with (for large pattern number) bank-type architectures are proposed for fully-parallel minimum distance search.**
- **Test chips are designed in 0.6μm (Hamming) and in 0.35μm CMOS technologies.**
- **Measured data indicates sufficient performance for application in mobile real-time systems.**